CLAIMS

What is claimed is:

1   1.   A data scrambler for a high density optical recording/reproducing apparatus, the

2   data scrambler comprising:

3   a random data generator which generates random data having a random data generation

4   cycle based on a result obtained by multiplying at least a size of a first data frame by a result

5   obtained by dividing a data amount of two tracks in an outermost circumference of the optical

6   disc by a size of a second data frame.

1   2.   The data scrambler of claim 1, wherein the size of the first data frame is one

2   sector, and the size of the second data frame is one error correction block.

1   3.   The data scrambler of claim 1, wherein the random data generation cycle is at

2   least as great as the result obtained by multiplying at least the size of the first data frame by the

3   result obtained by dividing the data amount of the two tracks in the outermost circumference of

4   the optical disc by the size of the second data frame.

1   4.   The data scrambler of claim 1, wherein the random data generator comprises:

2   registers, serially arranged, which shift-store n bits and generate random data, and uses

3   a total of n values as initial values, including a first initial value, first register values, which

4   are output after shifting the first initial value 7 times, a second initial value immediately after a

5   capacity required for return of the first initial value and the first register values, and second

6   register values which are output after shifting the second initial value 7 times; and

7   a first serial logic circuit having a plurality of logic gates, which exclusive-OR outputs

8   ones of the registers which correspond to a number of effective branches with a predetermined

9   branch value, and outputs of neighboring ones of the logic gates are fed back to a least

10   significant one of the registers,

11   wherein the data scrambler further comprises a second logic circuit which scrambles

12   outputs of a predetermined number of least significant ones of the registers and input data in

13   units of byte.

1   5.   The data scrambler of claim 4, wherein the random data generation cycle is 2^{16}

2   (=64 K) when n is 16.

1   6.   The data scrambler of claim 4, wherein the number of effective branches is at

2   least 4, and the effective branch value is any one of 8016h, 801Ch, 8029h, 80D0h, 810Ah,

3   810Ch, 8112h, 8142h, 8148h, 8150h, 8214h, 8241h, 8244h, 8248h, 8260h, 8320h, 8406h,

4   8430h, 8540h, 8580h, 8610h, 8805h, 8821h, 8841h, 8842h, 8920h, 8940h, 8A04h, 9028h,

5   9082h, 9120h, 9420h, 9840h, 9C00h, A084h, A101h, A108h, A140h, A440h, A801h, A840h,

6   B010h, B400h, C009h, C00Ah, C042h, C108h, C120h, C208h, C801h, CA00h, and D008h.

1   7.   The scrambler of claim 4, wherein the effective branch value is "B400h" and the

2   initial values include the first initial value as 0001h, the first register values as (0002h, 0004h,

3   0008h, 0010h, 0020h, 0040h, 0080h), which are obtained by left-shifting 0001h 7 times, the

4   second initial value as 7E80h, a result of the registers after 32K, which is the capacity required

5   for the return of the first initial and the first register values (B400h, 0002h, 0004h, 0008h,

6   0010h, 0020h, 0040h, 0080h), and the second register values as (FF01h, FE02h, FC04h,

7   F808h, F011h, E023h, C046h), which are obtained by left-shifting the second initial value

8   7E80h 7 times.

9   8.   The data scrambler of claim 1, wherein the random data generator comprises:

10   registers, serially arranged, which shift-store n bits and generate random data, and use

11   a total of n values as initial values, including a first initial value and register values, which are

12   supplied in each 4K times left-shifting of the first initial value,

13   a first serial logic circuit having a plurality of logic gates, which exclusive-ORs outputs

14   of ones of the registers which correspond to a number of effective branches with a

15 predetermined branch value, and outputs of neighboring ones of the logic gates are fed back to

16 a least significant one of the registers,

17 wherein the data scrambler further comprises a second logic circuit which scramblers

18 outputs of a predetermined number of least significant ones of the registers and input data in

19 units of byte.

1 9. The data scrambler of claim 8, wherein the random data generation cycle is 2^{16}

2 (=64 K) when n is 16.

1 10. The data scrambler of claim 8, wherein the number of effective branches is at

2 least 4, and the effective branch value is any one of 8016h, 801Ch, 8029h, 80D0h, 810Ah,

3 810Ch, 8112h, 8142h, 8148h, 8150h, 8214h, 8241h, 8244h, 8248h, 8260h, 8320h, 8406h,

4 8430h, 8540h, 8580h, 8610h, 8805h, 8821h, 8841h, 8842h, 8920h, 8940h, 8A04h, 9028h,

5 9082h, 9120h, 9420h, 9840h, 9C00h, A084h, A101h, A108h, A140h, A440h, A801h, A840h,

6 B010h, B400h, C009h, C00Ah, C042h, C108h, C120h, C208h, C801h, CA00h, and D008h.

1 11. The data scrambler of claim 8, wherein the value of the effective branch is

2 "B400h" and the initial values include the first initial value as 0001h and the register values as

3 (3DADh, D4E7h, FDCAh, EBCCh, 292Eh, 50F0h, BFCAh, 7F80h, D36Eh, BB39h, 5DFFh,

4 A809h, 6647h, 8044h, 0304h), which are obtained after every 4096 times left-shifting of the

5 first initial value 0001h.

1 12. The data scrambler of claim 1, wherein the random data generator changes the

2 effective branch value in units of a first cycle and generates a second cycle of the random data

3 according to a control value.

1 13. The data scrambler of claim 12, wherein the first cycle corresponds to an error

2 correction block and the second cycle corresponds to a sector.

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1   14.   The data scrambler of claim 12, wherein the second cycle is 4 K, and the

2   control value is one of 829h, 834h, 84Ch, 868h, 883h, 891h, 8B0h, 8C2h, 906h, 960h, 990h,

3   A03h, A18h, B04h, C48h, and CA0h in units of an error correction block.

1   15.   The data scrambler of claim 12, wherein the random data generator comprises:

2   a decoder which supplies 12 output bits, which correspond to 16 kinds of control

3   values, in units of an error correction block;

4   registers, arranged serially, which shifting-store 12 bits and generate random data in

5   units of a sector;

6   a selection output circuit which receives the 12 output bits supplied from the decoder,

7   as a selection signal, supplies a predetermined value for each bit of an effective branch among

8   the 12 output bits from the decoder, and otherwise supplies corresponding outputs of the

9   registers, to generate 12 outputs; and

10   a first logic circuit which exclusive-ORs the 12 output bit of the selection output circuit

11   and the 12 output bits of the registers and then, feeds back a result of the exclusive-ORing only

12   for each bit of the effective branch among the 12 output bits from the decoder,

13   wherein the data scrambler further comprises a second logic circuit which scrambles

14   outputs of a predetermined number of least significant ones of the registers and input data in

15   units of a byte.

1   16.   The data scrambler of claim 15, wherein initial values of the register are newly

2   set in each error correction block.

1   17.   A data scrambling method using a random data generator for a high density

2   optical recording/reproducing apparatus using an optical disc, the data scrambling method

3   comprising:

4   generating random data having a random data generation cycle based on a result by

5   multiplying at least a size of a first data frame by a result, which is obtained by dividing a data

6   amount of two tracks in an outermost circumference of the optical disc by a size of a second

7   data frame.

1   18.   The data scrambling method of claim 17, wherein the size of the first data frame

2   is a sector, and the size of the second data frame is an error correction block.

1   19.   The data scrambling method of claim 17, wherein the random data generation

2   cycle is at least as great as the result obtained by multiplying at least the size of the first data

3   frame by the result obtained by dividing the data amount of the two tracks in the outermost

4   circumference of the optical disc by the size of the second data frame.

1   20.   The data scrambling method of claim 17, wherein the generating of the random

2   data comprises shift-storing, n bits in registers and then, generating random data, wherein a

3   total of n values are used as initial values, including a first initial value, first register values,

4   which are obtained by shifting the first initial value 7 times, a second initial value immediately

5   after a capacity required for return of the first initial value and the first register values, and

6   second register values, which are obtained by shifting the second initial value 7 times,

         wherein the data scrambling method further comprises exclusive-ORing outputs of a

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8   predetermined number of least significant ones of the registers and input data in units of byte .

1   21.   The data scrambling method of claim 17, wherein the generating of the random

2   data comprises shift-storing n bits in registers and then, generating random data, wherein a

3   total of n values are used as initial values, including a first initial value and register values

4   which are supplied in each 4K times left-shifting of the first initial value;

5   wherein the data scrambling method further comprises exclusive-ORing outputs of a

6   predetermined number of least significant ones of the registers and input data in units of bit.

1   22.   The data scrambling method of claim 17, wherein the generating of the random

2   data comprises newly setting initial values in units of an error correction block of registers

3   generating random data in units of a sector, corresponding to 16 kinds of control values

4   supplied in units of the error correction block,

5   wherein the data scrambling method further comprises exclusive-ORing outputs of a

6   predetermined number of least significant ones of the registers and input data in units of byte .

1   23.   The data scrambler of claim 1, wherein:

2   the first data frame is approximately 4Kb (Kilobytes) in size;

3   the second data frame is approximately 64Kb in size; and

4   the data amount of the two tracks in the outermost circumference of the optical disc is

5   approximately 568Kb.

1   24.   The data scrambler of claim 1, wherein:

2   the first data frame is approximately 8Kb (Kilobytes) in size;

3   the second data frame is approximately 64Kb in size; and

4   the data amount of the two tracks in the outermost circumference of the optical disc is

5   approximately 568Kb.

1   25.   The data scrambler of claim 1, wherein:

2   the first data frame is approximately 4Kb (Kilobytes) in size;

3   the second data frame is approximately 128Kb in size; and

4   the data amount of the two tracks in the outermost circumference of the optical disc is

5   approximately 568Kb.

1   26.   The data scrambler of claim 1, wherein the random data generation cycle is at

2   least 64Kb (Kilobytes).

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1 27. The data scrambler of claim 4, wherein:

2   the size of the first data frame is a sector and the size of the second data frame is an

3 error correction block; and

4   the initial values are determined by an upper 4 bits of a last byte in a 4-byte

5 identification code which is allocated in each of a plurality of the first data frames.

1 28. The data scrambler of claim 8, wherein:

2   the size of the first data frame is a sector and the size of the second data frame is an

3 error correction block; and

4   the initial values are determined by an upper 4 bits of a last byte in a 4-byte

5 identification code which is allocated in each of a plurality of the first data frames.

1 29. The data scrambler of claim 15, wherein:

2   the size of the first data frame is a sector and the size of the second data frame is an

3 error correction block; and

4   the initial values are determined by an upper 4 bits of a last byte in a 4-byte

5 identification code which is allocated in each of a plurality of the first data frames.

1 30. The data scrambler of claim 1, wherein the random data generator:

2   a decoder to selectively output n bits as valid and invalid bits in response to input m

3 bits;

4   n registers arranged in serial, which shift and store the n bits, to generate shifted n bits

5 as the random data;

6   a selection circuit which selects a predetermined value or the shifted n bits for ones of

7 the shifted n bits, to generate a selection signal; and

8   logic gates arranged in serial, which perform XOR operations on the ones of the shifted

9 n bits, the ones of the shifted n bits, and an output of an adjacent more significant one of the

10 logic circuits, wherein the output of the logic gate associated with a least significant of the ones

11 of the shifted n bits is fed back to a least significant one of the registers.

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1   31.   The data scrambler of claim 30, further comprising:

2   a scrambling circuit which performs XOR operations on a plurality of least significant

3   ones of the shifted n bits and corresponding input data bits after the n registers 8-bit left shift

4   the n bits.

1   32.   The data scrambler of claim 30, further comprising:

2   a scrambling circuit which performs XOR operations on a plurality of least significant

3   ones of the shifted n bits and corresponding input data bits after each one-bit left shift of the n-

4   registers.

1   33.   The data scrambler of claim 30, further comprising:

2   a scrambling circuit which performs XOR operations on a plurality of least significant

3   ones of the shifted n bits and corresponding input data bits after the n registers 4k left shift the

4   n bits.

1   34.   The data scrambling method of claim 20, wherein:

2   the size of the first data frame is a sector and the size of the second data frame is an

3   error correction block; and

4   the method further comprising determining the initial values by an upper 4 bits of a last

5   byte in a 4-byte identification code which is allocated in each of a plurality of the first data

6   frames.

1   35.   The data scrambling method of claim 21, wherein:

2   the size of the first data frame is a sector and the size of the second data frame is an

3   error correction block; and

4   the method further comprising determining the initial values by an upper 4 bits of a last

5   byte in a 4-byte identification code which is allocated in each of a plurality of the first data

6   frames.

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1   36.   The data scrambling method of claim 17, wherein the generating of the random

2   data comprises shift-storing n bits in registers and then, generating random data, wherein a

3   total of n values are used as initial values, including a first initial value and register values,

4   which are supplied in each 4K left-shifting of the first initial value;

5   wherein the data scrambling method further comprises supplying exclusive-ORing

6   outputs of a predetermined number of least significant ones of the registers and input data in

7   units of byte.

1   37.   The data scrambling method of claim 17, wherein the generating of the random

2   data comprises:

3   selectively outputting n bits as valid and invalid bits in response to input m bits;

4   shifting and storing the n bits in serially arranged registers, to generate shifted n bits as

5   the random data;

6   selecting a predetermined value or the shifted n bits for ones of the shifted n bits, to

7   generate a selection signal; and

8   performing XOR operations on the ones of the shifted n bits, the ones of the shifted n

9   bits, and an output of an adjacent more significant one of the logic circuits, and feeding back

10 the output associated with a least significant of the ones of the shifted n bits to a least

11 significant one of the registers.

1   38.   The data scrambling method of claim 37, further comprising:

2   performing XOR operations on a plurality of least significant ones of the shifted n bits

3   and corresponding input data bits after 8-bit left-shifting the n bits in the n registers.

1   39.   The data scrambling method of claim 37, further comprising:

2   performing XOR operations on a plurality of least significant ones of the shifted n bits

3   and corresponding input data bits after one-bit left shifting of the n bits in the n registers; and

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4   repeating the performing of the XOR operations on the plurality of least significant

5   ones of the shifted n bits and the corresponding input data bits after each of repeated one-bit

6   left shifting of the n bits in the n registers.

1   40.   The data scrambling method of claim 37, further comprising:

2   performing XOR operations on a plurality of least significant ones of the shifted n bits

3   and corresponding input data bits after left shifting 4K times the n bits in the n registers.

1   41.   A data scrambler for a high density optical recording and/or reproducing

2   apparatus using an optical disc, comprising:

3   a random data generator which generates random data and adjusts a random data

4   generation cycle of the random data based upon a data amount of two tracks in an outermost

5   circumference of the optical disc; and

6   a scrambling circuit to scramble the random data.

1   42.   The data scrambler of claim 41, wherein the optical disc has error correction

2   blocks each comprising sectors, wherein:

3   the random data generator adjusts the random data generation cycle of the random data

4   based upon the size of each sector and a size of each error correction block.

1   43.   A data scrambler for a high density optical recording and/or reproducing

2   apparatus using an optical disc, comprising:

3   a random data generator which generates random data and adjusts a random data

4   generation cycle of the random data based upon a data amount in an innermost circumference

5   of the optical disc; and

6   a scrambling circuit to scramble the random data.

1   44.   The data scrambler of claim 43, wherein the optical disc has error correction

2   blocks each comprising sectors, wherein:

3   the random data generator adjusts the random data generation cycle of the random data

4   based upon the size of each sector and a size of each error correction block.

1   45.   A data scrambler for a high density optical recording and/or reproducing

2   apparatus using an optical disc having error correction blocks each comprising sectors, the data

3   scrambler comprising:

4   a random data generator which generates random data and adjusts a random data

5   generation cycle of the random data based upon a size of each sector and a size of each error

6   correction block; and

7   a scrambling circuit to scramble the random data.

1   46.   A data scrambler for a high density optical recording and/or reproducing

2   apparatus using an optical disc having second data frames each comprising a plurality of first

3   data frames, the data scrambler comprising:

4   a random data generator which generates random data and adjusts a random data

5   generation cycle of the random data based upon a size of each first data frame and a size of

6   each second data frame; and

7   a scrambling circuit to scramble the random data.